We Claim:

1. In a manufacturing process for a memory cell array of a semiconductor component, the component having:

a substrate with a surface, bit lines formed in the surface of the substrate by introduction of dopant, and strip-type word lines formed on the surface of the substrate;

the word lines extending parallel to one another and transversely with respect to the bit lines, forming gate electrodes in each case between the bit lines, and having an insulation layer of silicon oxide and a silicon nitride cover layer disposed thereon; and

spacers of silicon oxide disposed alongside at sidewalls of the word lines;

a method for fabricating self-aligned contacts to the bit lines, the method which comprises:

forming a silicon nitride layer on the spacers and on the cover layer and filling spaces between the word lines with a filling;

leveling the filling and thereby uncovering the silicon nitride layers on the word lines during leveling of the

filling and removing the silicon nitride layers by etching selectively with respect to the silicon oxide layers to form openings;

subsequently expanding the openings laterally by etching the silicon oxide layers selectively with respect to residual portions of the silicon nitride layer on the spacers; and

subsequently filling the holes with silicon nitride to form coverings of silicon nitride projecting laterally above the word lines.

2. The method according to claim 1, which comprises fabricating a storage layer sequence for charge trapping of hot electrons from a respective channel region and for serving as a storage layer.

3. The method according to claim 1, which comprises filling the spaces between the word lines with borophosphoro-silicate glass.

4. The method according to claim 3, wherein the word lines comprise silicon-containing material, and the method further comprises, prior to fabricating the spacers of oxide, oxidizing a material of the word lines to form an oxide layer encapsulating the word lines.